40V 5.9mohmN-channel SGTMOSFET

SI059N04MG2

Description:

This N channel SGT MOSFET has been designed to ultra-low on-state resistance (R_{DSON}) and yet maintain superior switching performance, special for high efficiency power management applications.

Features:

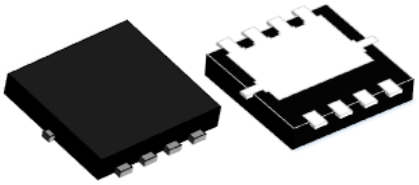
- N-channel, optimized for high-speed smooth switching
- Excellent Gate Charge × R_{DSON} (FOM)
- Ultra-low on-resistance
- RoHS compliant (Note 1)
- Halogen-free (Note 1)

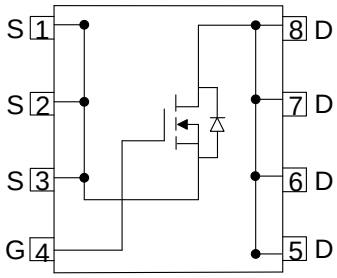
Applications:

- DC-DC Converter
- Power Tools
- Load Switching

Key Performance Parameters:

Parameter	Value	Unit
V_{DS}	40	V
$R_{DSON,\ max}$ @VGS=10V	5.9	mΩ
I_D	54	A





Ordering Information:

Ordering Code	Package Type	Marking Code	Form	Packing
SI059N04MG2	DFN3.3X3.3-8L	059N04M	13 inches Reel	5000

Maximum Ratings(T_A = 25℃ unless otherwise noted)

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	40	V
I_D	Drain Current - Continuous (T_C = 25°C)	54	A
	Drain Current -Continuous (T_C = 100°C)	34	A
I_{DM}	Drain Current - Pulsed (Note 1,2)	216	A
V_{GS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 3)	56	mJ
P_D	Power Dissipation (T_C = 25°C)	36.7	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	ºC

Thermal Characteristics

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Steady-State	3.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Steady State (Note 4)	60.4	°C/W

Notes:

1. The max drain current rating is package limited
2. Repetitive Rating: Pulse width limited by maximum junction temperature
3. L = 0.5 mH, V_{DD} = 20V, I_{AS} = 14.7A, R_G = 25 Ω, Starting T_J = 25 °C
4. Mount on minimum PCB layout

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V, T_J = 25℃			1	μA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 150℃			250	
I_{GSS}	Gate Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
$V_{GS(TH)}$	Gate Threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	1.1	1.6	2.1	V
$R_{DS(On)}$	Drain-Source on-state resistance	V_{GS} = 10 V, I_D = 20A		5.0	5.9	mΩ
		V_{GS} = 4.5 V, I_D = 15A		7	8.5	
Dynamic Characteristics						
C_{ISS}	Input capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1.0 MHZ		850		pF
C_{OSS}	Output capacitance			254		pF
C_{RSS}	Reverse transfer capacitance			8		pF
R_G	Gate resistance	f = 1MHZ		26		Ω
Switching Characteristics						
$T_{D(ON)}$	Turn On Delay Time	V_{DS} = 20 V, I_D = 20 A, V_{GS} = 10 V, R_{GEN} = 10 Ω (Note 5)		7		ns
T_R	Rising Time			52.5		ns
$T_{D(OFF)}$	Turn Off Delay Time			44.5		ns
T_F	Fall Time			93.5		ns
Q_G	Total Gate Charge	V_{DS} = 20 V, I_D = 20 A, V_{GS} = 10 V		13.1		nC
Q_{GS}	Gate-Source Charge			2.2		nC
Q_{GD}	Gate-Drain Charge			2.6		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Body-Diode Forward Current				54	A
I_{SM}	Maximum Pulsed Body-Diode Forward Current (NOTE 1)				216	A
V_{SD}	Diode Forward Voltage	V_{GS} = 0 V, I_S = 20 A		0.84		V
T_{RR}	Reverse recovery time	I_F = 40 A, di/dt = 100 A/μS		24.5		ns
Q_{RR}	Reverse recovery charge			14		nC

Electrical Characteristics Diagrams

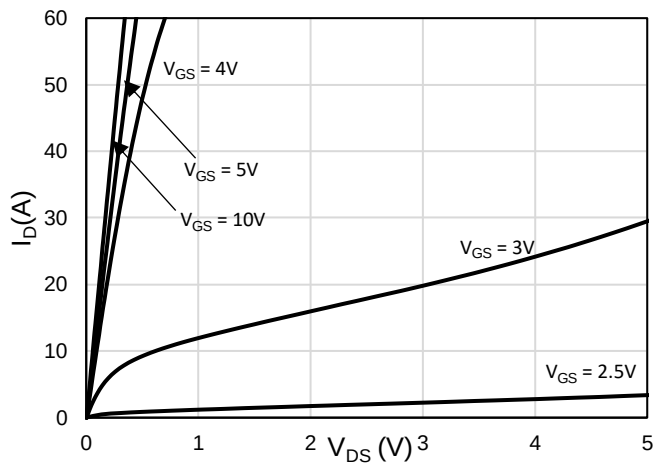


Figure 1: On-Region Characteristics

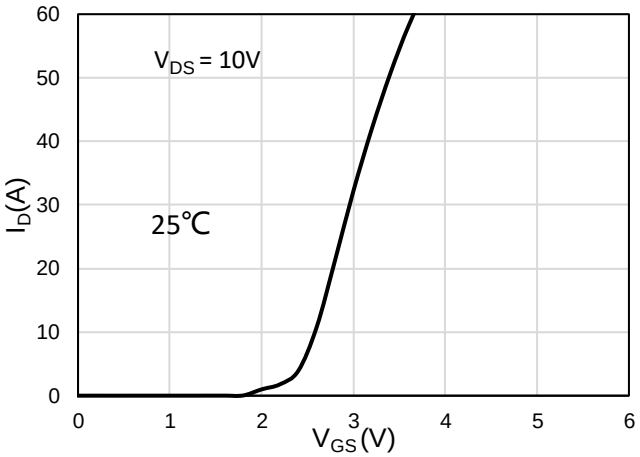


Figure 2: Transfer Characteristics

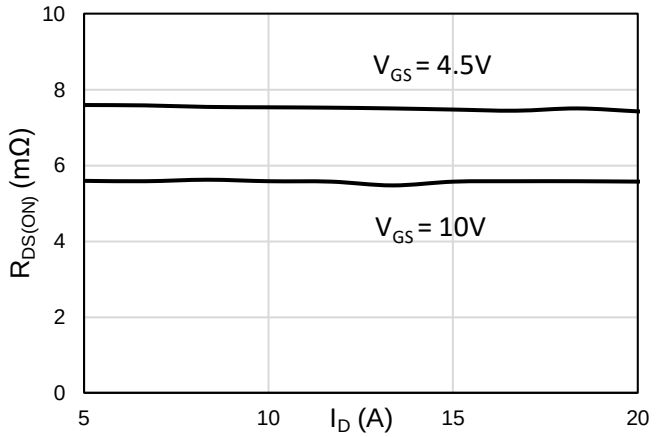


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

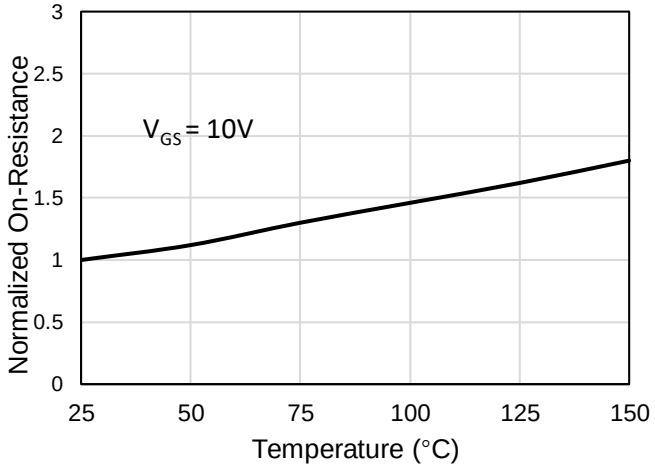


Figure 4: On-Resistance vs. Junction Temperature

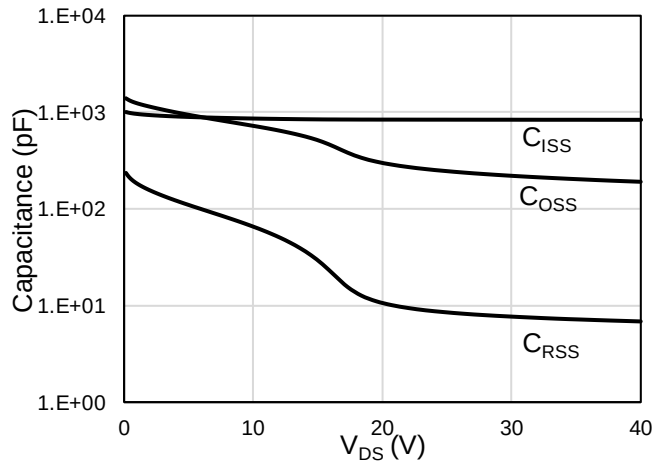


Figure 5: Capacitance Characteristics

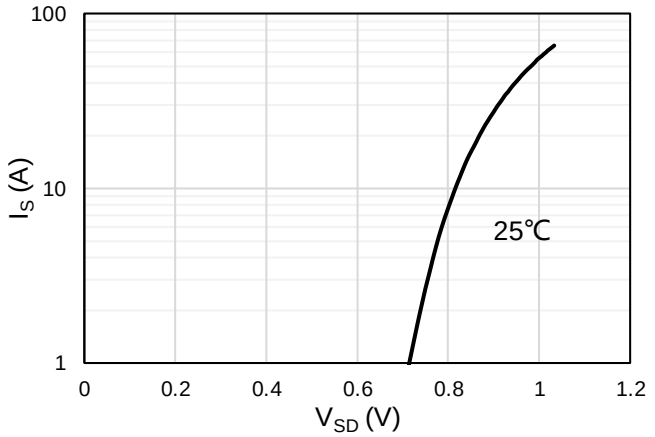


Figure 6: Body-Diode Characteristics

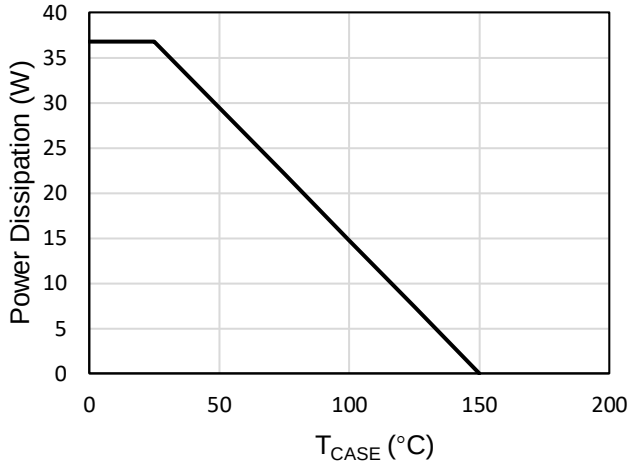


Figure 7: Power De-rating

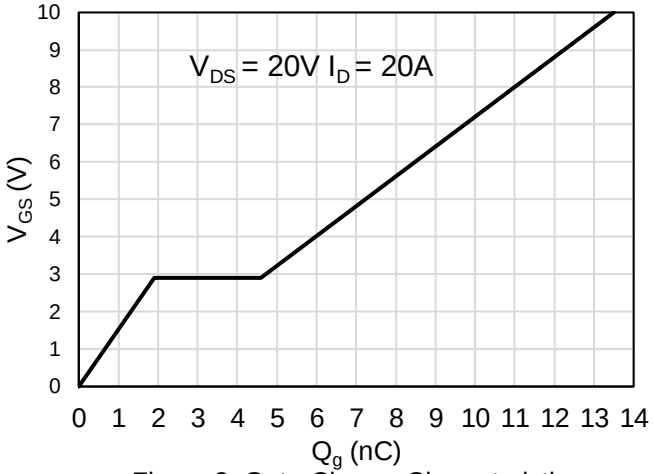


Figure 8: Gate-Charge Characteristics

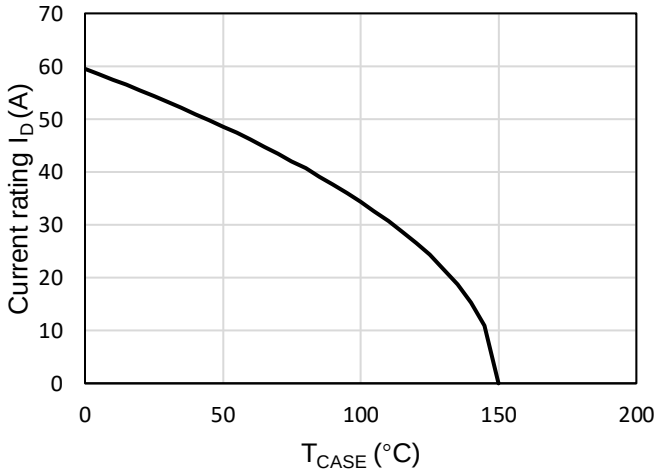


Figure 9: Current De-rating

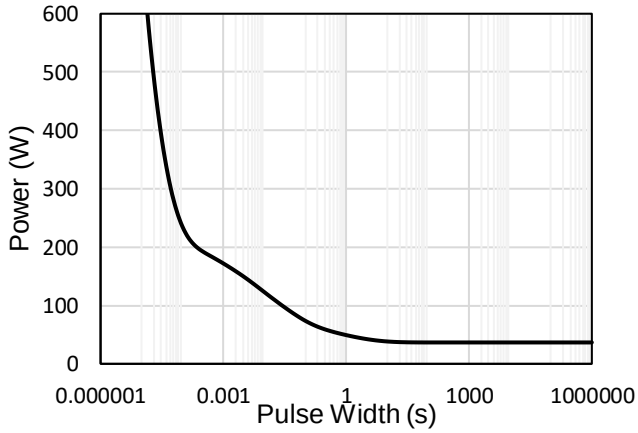


Figure 10: Single Pulse Power Rating Junction-to-Case

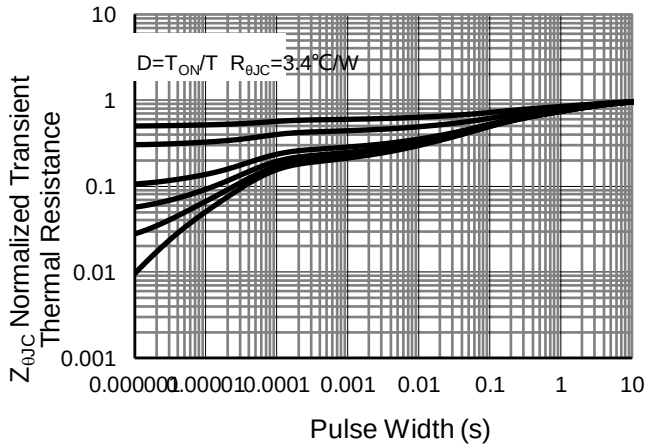


Figure 11: Normalized Maximum Transient Thermal Impedance

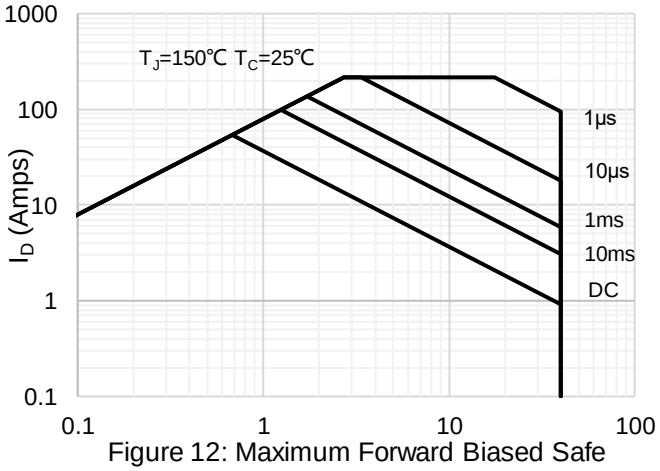


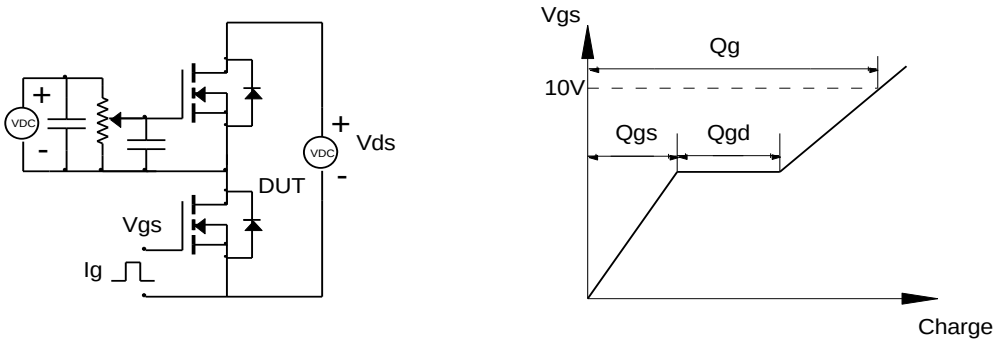
Figure 12: Maximum Forward Biased Safe Operating Area

Notes:

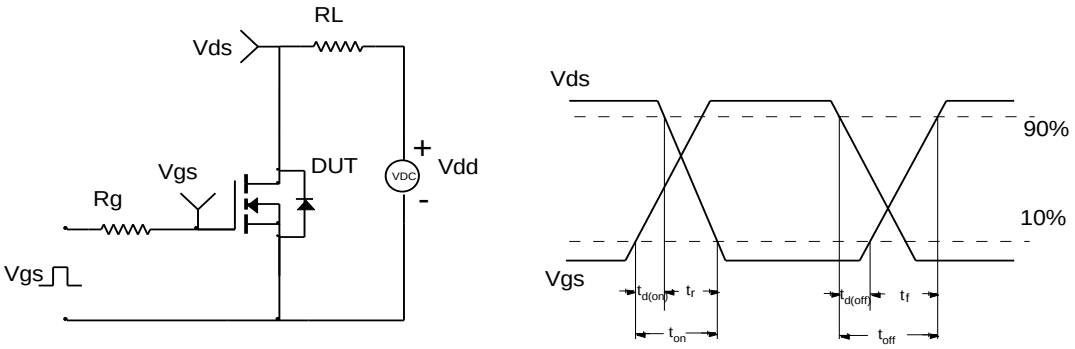
1. Pulse Test: Pulse width ≤ 300 us, Duty cycle ≤ 2%
2. Essentially independent of operating temperature

Test Circuit and Waveform

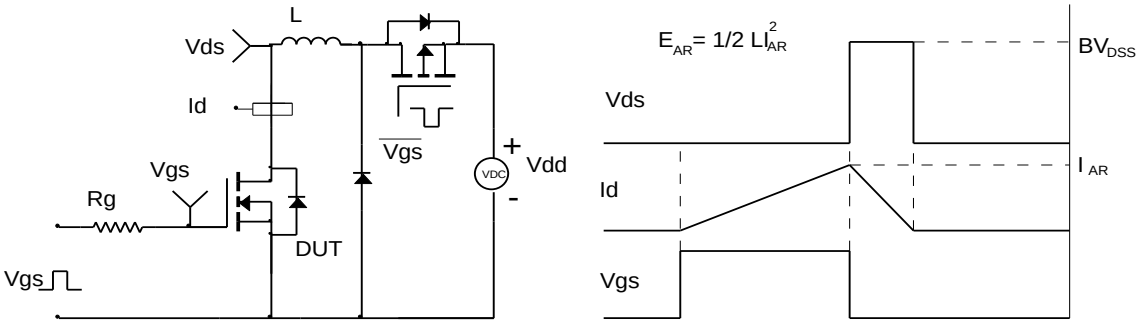
Gate Charge Test Circuit & Waveform



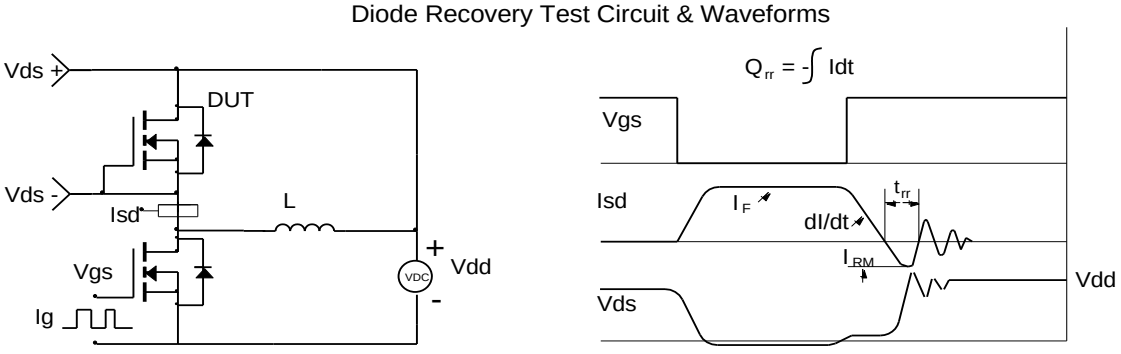
Resistive Switching Test Circuit & Waveforms



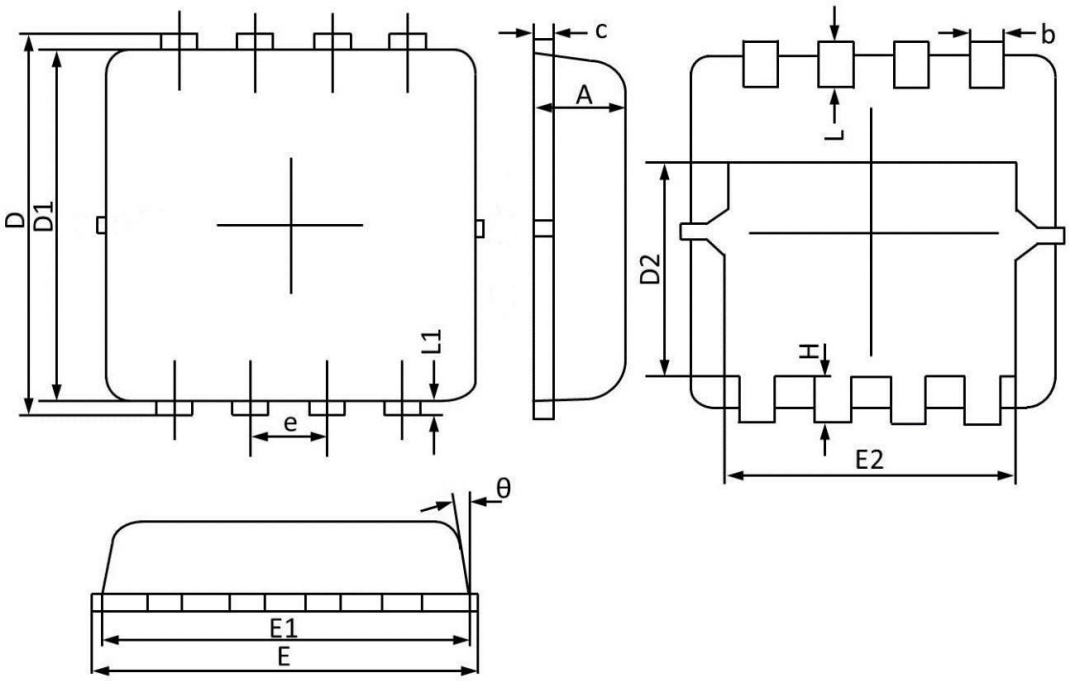
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outlines



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MAX	MIN	MAX	MIN
A	0.900	0.700	0.035	0.028
b	0.350	0.250	0.014	0.010
c	0.250	0.100	0.010	0.004
D	3.500	3.050	0.138	0.120
D1	3.200	2.900	0.126	0.114
D2	1.950	1.350	0.077	0.053
E	3.400	3.000	0.134	0.118
E1	3.300	2.900	0.130	0.114
E2	2.600	2.350	0.102	0.093
e	0.65BSC		0.026BSC	
H	0.750	0.300	0.030	0.012
L	0.600	0.300	0.024	0.012
L1	0.200	0.060	0.008	0.002
θ	14°	6°	14°	6°